UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,640	07/29/2003	Maher Amer	13587.39	6843

43831 7590 04/24/2007

BERKELEY LAW & TECHNOLOGY GROUP, LLP
1700 NW 167TH PLACE
SUITE 240
BEAVERTON, OR 97006

EXAMINER	
LAFORGIA, CHRISTIAN A	
ART UNIT	**PAPER NUMBER**
2131	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,640	AMER, MAHER	
	Examiner	Art Unit	
	Christian La Forgia	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment of 22 February 2007 has been noted and made of record.

2. Claims 1-16 have been presented for examination

Response to Arguments

3. Applicant's arguments, see page 6, filed 22 February 2007, with respect to the drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn.

4. Applicant's arguments filed 22 February 2007 have been fully considered but they are not persuasive.

5. The Examiner disagrees with the Applicant's mischaracterization of the previous Office Action alleging that the Examiner rejected claims 9-11 under 35 U.S.C. 102(b). As noted in paragraph 19, which is the paragraph outlining which claims are rejected under 35 U.S.C. 103(a), it can be seen that claims 9-11 have been included in said heading and have therefore been rejected under 35 U.S.C. 103(a). Likewise in paragraph 6, which lists those claims that have been rejected under 35 U.S.C. 102(b), there is no mention of claims 9-11, thereby presenting no prima facie anticipation rejection of claims 9-11. The Examiner was attempting to keep the Office Action concise by grouping identical claims; the Examiner was grouping the claims for the sake of brevity and clarity, namely to prevent repeating the identical rejection in two different locations in the Office Action.

6. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

7. In response to the Applicant's arguments on page 7 regarding claim 1 that Lee fails to disclose the determination and generation of the appropriate subset wherein, for each bit of the set of data bits, at least one bit of the appropriate subset is associated therewith, the Examiner disagrees. As noted in the previous Office Action, and again below, Lee discloses, in a related document, on at least page 1053 of the IEEE publication entitled "Realizations of Parallel and Multibit-Parallel Shift Register Generators" that the parallel scrambling disclosed in the instant invention has been modified to be multibit-parallel scrambling. This is further supported by at least figures 4, 5, and 6A, all cited in the rejection of the claim limitation in question.

8. The Examiner disagrees with the Applicant's arguments on page 7, that the reliance on the IEEE article by Lee is misplaced. The applicant's argument appear to be based upon the time discrepancy of the references, while it has been held that contentions that the references are unrelated due to the time gap are not impressive. See *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977). First, it is clear that the IEEE article has the same authors and is directed toward the same subject matter as the prior art reference applied. Aside from the coincidence that the authors/inventors and subject matter is the same, the figures disclosed in the IEEE document are similar to the patent applied to the claims of the instant invention; for example, Figure 1(a) of the cited IEEE document is drawn to figures 2A and 2B of U.S. Patent No. 5,355,415. Likewise Figure 1(b) of the cited IEEE document is similar to figures 6A and 6B of U.S. Patent No. 5,355,415. Finally, the IEEE document was published in 1997, which is still 5 years prior to the Applicant's claim to priority to U.S. Provisional Application 60/411,343.

9. The Examiner further disagrees with the Applicant's arguments on page 7 in stating that the anticipation rejection based on this article is flawed and improper. When a references is "to

serve as an anticipation when the reference is silent about the asserted inherent characteristic, such a gap in the reference may be filled with recourse to extrinsic evidence[;] such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." See MPEP § 2131.01(III); see also *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). In using the IEEE document the Examiner was filling a gap that the patent reference was silent about that were otherwise inherent to the invention.

10. In response to the Applicant's arguments on page 8 regarding claim 13, that Lee fails to disclose the determination and generation of the appropriate subset wherein, for each bit of the set of data bits, at least one bit of the appropriate subset is associated therewith by performing a bitwise parallel exclusive-OR, the Examiner disagrees. As noted in the previous Office Action, and again below, Lee discloses, in a related document, on at least page 1058 of the IEEE publication entitled "Realizations of Parallel and Multibit-Parallel Shift Register Generators" that the parallel scrambling disclosed in the instant invention has been modified to be multibit-parallel scrambling using an exclusive-OR operation. This is further supported by at least figures 2A, 2B, 3A, 3B, 6A, 6B, 8A and 8B which illustrate the symbol ⊕, which is understood in logical terms to represent the exclusive-OR operation, as cited below. Furthermore, Lee's IEEE reference states that for Figure 9, ⊕ represents a modulo-2 adder. As noted above, the use of exclusive-OR operations is further supported by page 1058 of Lee's disclosure in the IEEE publication.

11. In response to the Applicant's argument on page 9, regarding claim 8, that Amrany does not disclose selection means for selecting between a first set of data bits to be scrambled and a

second set of data bits to be descrambled, the Examiner disagrees. Amrany discloses at column 4, lines 24-53, that the selector couples the output of the inverter or the output of the exclusive-OR gate to the shift register when the system is used for scrambling. Likewise, the selector, via a signal from a lead, couples either the received scrambled data or the output of the inverter into the shift register, thereby descrambling the data. Therefore, Amrany discloses a selection means for selecting between scrambling a data set or descrambling a data set.

12. See further rejections that follow.

Claim Rejections - 35 USC § 102

13. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

14. Claims 1-7 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,355,415 to Lee et al., hereinafter Lee.

15. As per claim 1, Lee teaches a system for processing a set of data bits using a subset of a recurring sequence of scrambler bits, the system comprising:

receiving means for receiving said set of data bits (Figures 3B [input line for $\{b_k\}$], 4, column 4, lines 41-44, i.e. input data sequence);

storage means for storing said set of data bits (Figures 3B [input lines for $\{b^0_k, b^1_k, b^{n-1}_k,\}$], 4, 6A [input lines for data sequence $\{b^0_k, b^1_k, b^{n-1}_k,\}$], column 4, lines 55-57, i.e. parallel input data sequences);

digital logic means for determining an appropriate subset of said sequence of scramble bits based, at least in part, on a generator polynomial and one or more bits from a prior

appropriate subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

generating means for generating said appropriate subset based, at least in part, on said generator polynomial and said prior appropriate subset wherein, for each bit of said set of data bits, at least one bit of said appropriate subset is associated therewith (Figures 4, 5, 6A [blocks 61, 72], 8B, column 6, lines 17-20, column 10, lines 6-51, i.e. generating parallel sequences for scrambling parallel input data sequences); and

digital operation means for performing a bitwise parallel digital operation between each bit of said set of data bits and said at least one bit of said appropriate subset associate therewith to produce an output set of data bits (Figures 3B, 4, 5, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences). Lee discloses on at least page 1053 of the IEEE publication entitled "Realizations of Parallel and Multibit-Parallel Shift Register Generators" that the parallel scrambling disclosed in the instant invention has been modified to be multibit-parallel scrambling.

16. Regarding claim 2, Lee teaches wherein said system scrambles said set of data bits using said appropriate subset of scramble bits (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences).

17. Regarding claim 3, Lee teaches wherein said system descrambles said set of data bits using said appropriate subset of scramble bits (Figure 6B [block 69], column 6, lines 30-57).

18. Regarding claims 4 and 10, Lee teaches wherein said receiving means comprises a multiplexer (column 4, lines 41-44, i.e. the input data sequence $\{b_k\}$ should be multiplexed to implement parallel distributed scrambling).

19. Regarding claim 5, Lee teaches wherein said digital logic means determines said appropriate subset based on an immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from D.W. Choi's publication "Parallel scrambling techniques for digital multiplexer," hereinafter Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

20. With regards to claims 6 and 11, Lee teaches wherein said digital logic means is a combinational logic circuit (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. shift register).

21. Regarding claims 7 and 9, Lee teaches wherein said bitwise parallel operation is a bitwise parallel XOR operation (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20). The symbol ⊕ disclosed in Figures 2A, 2B, 3A, 3B, 6A, 6B, 8A and 8B is understood in logical terms to represent the exclusive-OR operation. The Lee reference states that for Figure 9, ⊕ represents a modulo-2 adder.

22. As per claim 13, Lee teaches a method of processing a plurality of data bits using a subset of a recurring sequence of scrambler bits, the method comprising:

a) receiving (Figures 3B [input line for $\{b_k\}$], 4, column 4, lines 41-44, i.e. input data sequence) and storing in parallel said plurality of data bits (Figures 3B [input lines for $\{b^0_k, b^1_k, b^{n-1}_k,\}$], 4, 6A [input lines for data sequence $\{b^0_k, b^1_k, b^{n-1}_k,\}$], column 4, lines 55-57, i.e. parallel input data sequences);

b) determining an appropriate subset of said sequence of scrambler bits based on an immediately preceding subset of said sequence of scrambler bits(Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

c) generating said appropriate subset wherein, for each bit of said plurality of data bits, at least one bit of said appropriate subset is associated therewith (Figures 6A [blocks 61, 72], 8B, column 6, lines 17-20, column 10, lines 6-51, i.e. generating parallel sequences for scrambling parallel input data sequences);

d) loading said appropriate subset in a storage means (column 6, lines 24-28, i.e. the parallel sequences are obtained from the parallel shift register generator); and

e) performing a bitwise parallel XOR operation between each bit of said plurality of data bits and said at least one bit of said appropriate subset associated therewith to produce an output set of data bits (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state). The symbol ⊕ disclosed in Figures 2A, 2B, 3A, 3B, 6A, 6B, 8A and 8B is understood in logical terms to represent the exclusive-OR operation. The Lee reference states that for Figure 9, ⊕ represents a modulo-2 adder. The use of exclusive-OR operations is further supported by page 1058 of Lee's disclosure in the IEEE publication entitled "Realizations of Parallel and Multibit-Parallel Shift Register Generators."

23. Regarding claim 14, Lee teaches wherein step b) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next

state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

24. Regarding claim 15, Lee teaches wherein step c) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset (column 6, line 66 to column 7, line 2, i.e. the parallel sequence generating vector). Lee states at column 6, line 66 to column 7, line 2 that the parallel sequence generating vector can be obtained from Choi. Choi states on pages 124 and 125 that parallel sequence generating vector basis the next parallel sequence on the current parallel sequence.

25. Regarding claim 16, Lee teaches wherein said storage means is a register (column 6, lines 24-28, i.e. the parallel sequences are obtained from the parallel shift register generator).

Claim Rejections - 35 USC § 103

26. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

27. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of U.S. Patent No. 5,530,959 to Amrany, hereafter Amrany.

28. As per claim 8, Lee teaches a digital scrambler/descrambler using a subset of a securing sequence of scrambler bits, the scrambler/descrambler comprising:

digital logic means for determining an appropriate subset of said sequence of scrambler bits, said appropriate subset being determined based on an immediately preceding subset of said

sequence of scrambler bits (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

digital operation means for executing a bitwise parallel digital operation between said appropriate subset and said data set (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

29. Lee does not teach selection means for selecting between a first set of data bits to be scrambled and a second set of data bits to be descrambled.

30. Amrany discloses a selection means (Figures 4 [blocks 408, 428], 5 [block 428], 6 [block 428], column 3, lines 40-59, column 4, lines 24-53).

31. Lee and Amrany are related in their field of endeavors as they are both related to self-synchronizing scrambling of data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the selection means of Amrany in the system of Lee, since Amrany states at column 3, lines 37-39 that using a selector avoids using synchronization signals which are difficult and expensive to implement, especially in high speed communications.

32. With regards to claim 12, Lee teaches wherein said digital logic means includes a digital storage means for storing said immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. shift register).

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (571) 272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian LaForgia
Patent Examiner
Art Unit 2131

clf

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100